a

140 MSPS Graphics Digitizer

Preliminary Technical Data 1/27/99 AD9884

The AD9884 is a complete 8-bit 140MSPS, monolithic graphics digitizer optimized for digitizing RGB graphics signals from personal computers and workstations. Its 140MSPS encode rate capability and full-power analog bandwidth of 500MHz supports display resolutions of up to 1280 x 1024 at 75Hz with sufficient input bandwidth to accurately acquire and digitize each pixel.

To minimize system cost and power dissipation, the AD9884 includes an internal +1.25V reference, PLL to generate a pixel clock from HSYNC and COAST, and programmable gains, offset, and clamp control. The user provides only a +3.3V power supply, analog input, and HSYNC and COAST signals. Three-state CMOS outputs may be powered from 2.5V to 3.3V.

The AD9884's on-chip PLL generates a pixel clock from HSYNC and COAST inputs. Pixel clock output frequencies range from 20 to 140 MHz. PLL clock jitters is 500ps p-p typical relative to the input reference. When the COAST signal is presented, the PLL maintains its output frequency in the absence of HSYNC. A sampling phase adjustment is provided. Data, HSYNC and Clock output phase relationships are maintained. The PLL can be disabled and external clock input provided as the pixel clock.

A clamp signal is generated internally or may be provided by the user through the CLAMP input pin. This device is fully programmable via a two wire serial port.

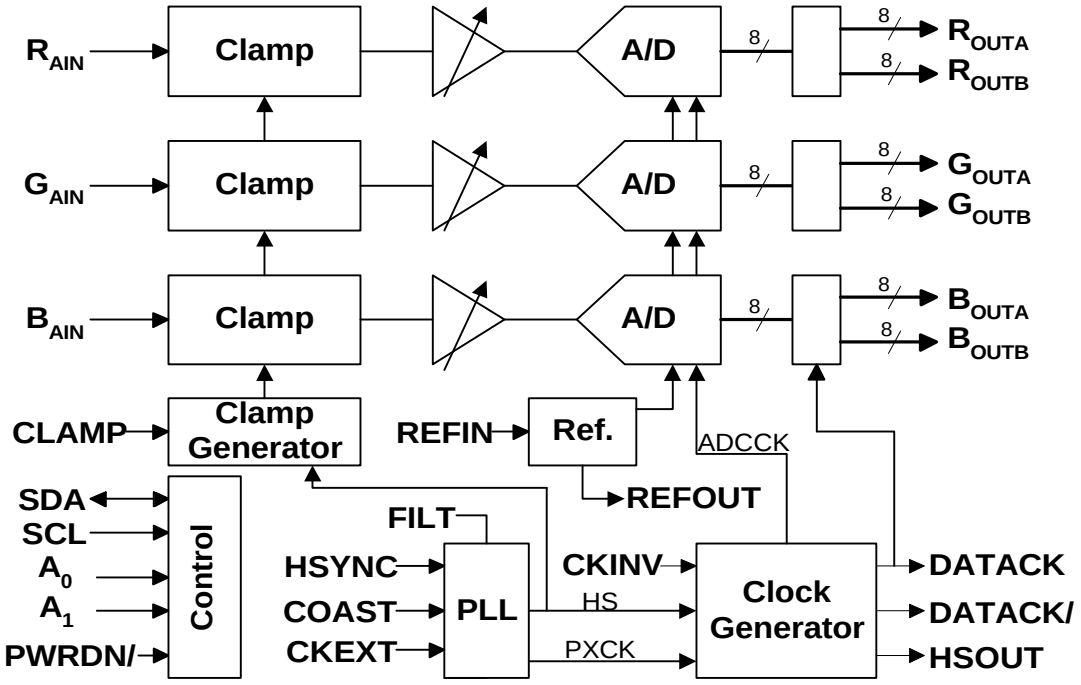
Fabricated in an advanced CMOS process, the AD9884 is provided in a space-saving 128-lead MQFP surface mount plastic package and is specified over the 0°C to +85°C temperature range.

FEATURES
140 MSPS Maximum Conversion Rate
500 MHz Analog Bandwidth
0.5V to 1.0V Analog Input Range
500pS p-p PLL clock jitter
3.3V power supply

2.5V to 3.3V three-state CMOS outputs
Demultiplexed Output Ports
Data Clock Output Provided
Low Power: 730mW Typical
Internal PLL generates CLOCK from HSYNC

Serial port interface
Fully programmable
Supports 2 pixels per clock mode

APPLICATIONS
RGB Graphics Processing
LCD Monitors and Projectors
Plasma Display Panels
Scan Converters



REV. PrA

One Technology Way, P.O Box 9106, Norwood, MA 02062–9106, USA
Tel: 617/329–4700 **Fax: 617–326–8703**

CRITICAL CHARACTERISTICS (V_D = +3.3V, V_{DD} = +3.3V, ADC Clock = Maximum conversion rate

Parameter	Test Temp	Level	AD9884KST-140 Min	AD9884KST-140 Typical	AD9884KST-140 Max	AD9884KST-100 Min	AD9884KST-100 Typical	AD9884KST-100 Max	Units
RESOLUTION				8			8		bits
DC ACCURACY									
Differential Nonlinearity	+25°C	I		0.5			0.5		LSB
	Full	VI		0.9			0.9		LSB
Integral Nonlinearity	+25°C	I		0.5			0.5		LSB
	Full	VI		0.9			0.9		LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed		
Gain Tempco	Full	V		TBD			TBD		ppm/°C
ANALOG INPUT									
Input Voltage Range	Full	V	0.5		1.0	0.5		1.0	V p–p
Input Resistance	+25°C	I		TBD			TBD		kΩ
	Full	VI		TBD			TBD		kΩ
Input Capacitance	+25°C	V		4			4		pF
Input Bias Current	+25°C	I		TBD			TBD		µA
	Full	VI		TBD			TBD		µA
HSYNC Input Range	Full	V	30		90	30		90	kHz
Analog Bandwidth, Full Power	+25°C	V		500			500		MHz
REFERENCE OUTPUT									
Output Voltage	Full	VI		+1.25			+1.25		V
Temperature Coefficient	Full	V		50			50		ppm/°C
SWITCHING PERFORMANCE									
Maximum Conversion Rate	Full	VI	140			100			MSPS
Minimum Conversion Rate	Full	IV			20			20	MSPS
Data to Clock Skew	Full	VI		TBD			TBD		ns
DIGITAL INPUTS									
Input Capacitance	+25˚C	V		3			3		pF
DIGITAL OUTPUTS									
Logic "1" Voltage	Full	VI	V_D-0.1			V_D-0.1			V
Logic "0" Voltage	Full	VI			0.1			0.1	V
Output Coding				Binary			Binary		
POWER SUPPLY									
V_D Supply Current	Full	VI		180			180		mA
V_{DD} Supply Current	Full	VI		40			40		mA
Total Power Dissipation	Full	VI		730			730		mW
Powerdown Supply Current	Full	VI		TBD			TBD		mA
Powerdown Dissipation	Full	VI		TBD			TBD		mW
DYNAMIC PERFORMANCE									
Transient Response	+25°C	V		2			2		ns
Overvoltage Recovery Time	+25°C	V		1.5			1.5		ns
Signal–to–Noise Ratio (SNR) (Without Harmonics)									
f_{IN} = 19.7 MHz	+25°C	I		46			46		dB
	Full	V		45			45		dB
Signal–to–Noise Ratio (SINAD) (With Harmonics)									
f_{IN} = 19.7 MHz	+25°C	I		45			45		dB
	Full	V		44			44		dB
Effective Number of Bits									
f_{IN} = 19.7 MHz	+25°C	I		7.2			7.2		bits
Crosstalk	Full	V		55			55		dBc

ORDERING GUIDE

Model	Temperature Range	Package Option
AD9884KS-140	0°C to +85°C	ST-128
AD9884KS-100	0°C to +85°C	ST-128
AD9884/PCB	+25°C	Evaluation Board

EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested.

II 100% production tested at +25°C and sample tested at specified temperatures.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at +25°C; guaranteed by design and characterization testing.

ABSOLUTE MAXIMUM RATINGS*

V_D ..... +4 V
V_{DD} ..... +4 V
Analog Inputs ..... V_D to 0.0 V
VREF IN ..... V_D to 0.0 V
Digital Inputs ..... V_D to 0.0 V
Digital Output Current ..... 20 mA
Operating Temperature ..... 0°C to +85°C
Storage Temperature ..... –65°C to +150°C
Maximum Junction Temperature ..... +175°C
Maximum Case Temperature ..... +150°C

- Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Serial Port Register Address List.

Note: All data is assumed to be loaded MSB first.

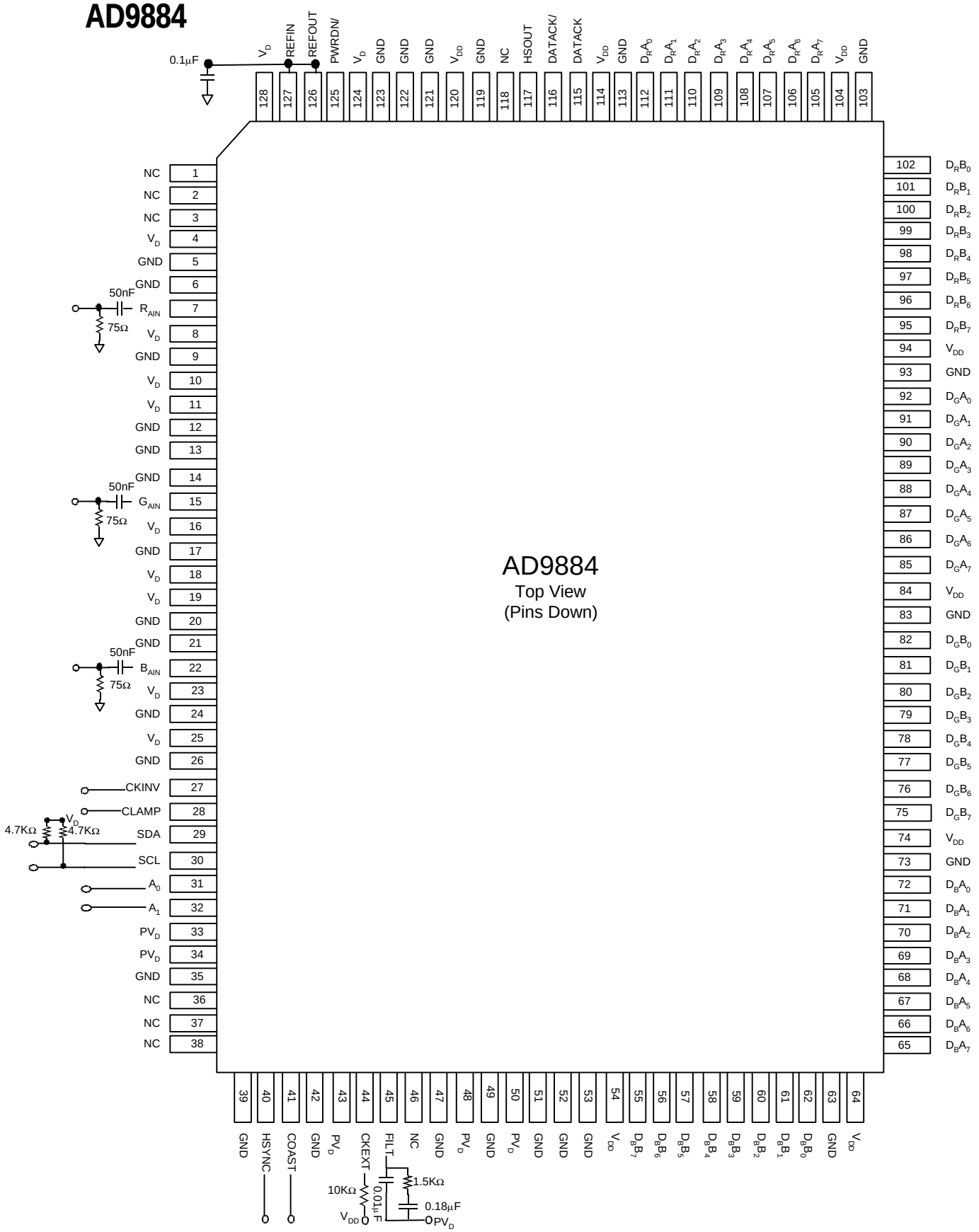
Hex Address	Bits	Register Name	Function
00H	7:0	PLL Div MSB	This register is for bits [11:4] of the PLL divider. Larger values mean the PLL operates at a faster rate. This register should be loaded first whenever a change is needed (This will give the PLL more time to lock.)
01H	7:4	PLL Div LSB	Bits [3:0] of the MSB divider word
02H	7:0	Red Gain	Controls ADC input range (Contrast) of each respective channel. Smaller values give more contrast.
03H	7:0	Green Gain	
04H	7:0	Blue Gain	
05H	7:2	Red Offset	Controls DC offset (Brightness) of each respective channel. Smaller values give a brighter image.
06H	7:2	Green Offset	
07H	7:2	Blue Offset	
08H	7:0	Clamp Placement	Places the Clamp signal an integer number of clock periods after the trailing edge of the HSYNC signal (See Control register Bit 3 description).
09H	7:0	Clamp Duration	Number of clock periods that the Clamp signal is actively clamping.
0AH	7:1	Control	Bit 7 – Channel Mode. Determines Single Channel or Dual Channel output mode. (Logic 0 selects Single Channel mode.)
			Bit 6 – Output Mode. Determine Interleaved or Parallel output mode. (Logic 0 selects Interleaved mode.)
			Bit 5 – HSYNC Polarity. Changes polarity of incoming HSYNC signal. (Logic 1 selects active high.)
			Bit 4 – Coast Polarity. Changes polarity of external COAST signal. (Logic 1 selects active high)
			Bit 3 – Clamp Function. Chooses between HSYNC for Clamp signal or another external signal to be used for clamping. (Logic 0 chooses HSYNC).
			Bit 2 – Clamp Polarity. Valid only with external CLAMP signal. Logic 1 selects active low.
			Bit 1 – PLL Bypass. Shuts down PLL and allows external clock to drive the part. (Logic 1 selects bypassing of the internal PLL.)
0BH	7:3	Phase Adjust	ADC Clock phase adjustment. Larger values mean more delay. (1LSB=T/32)
0CH	7:2	VCO/CPMP	Bit 7 – Must be set to 0 for proper device operation.
			Bits [6:5] VCO Range. Selects VCO frequency range. (see PLL description)
			Bits [4:2] Charge Pump Current. Varies the current that drives the low pass filter. (see PLL description)
0DH		Test Register	Reserved for future use

•

Serial Port Default Values

Register Name		Default Value
PLL Divider		1693
Red Gain		128
Green Gain		128
Blue Gain		128
Red Offset		32
Blue Offset		32
Green Offset		32
Clamp Placement		128
Clamp Duration		128
Control	Channel Mode	1 (Dual Channel Mode)
	Output Mode	1 (Parallel)
	HSYNC Polarity	1 (Active high)
	COAST Polarity	1 (Active high)
	Clamp Function	0 (Clamp derived from HSYNC)
	Clamp Polarity	1 (Active low)
	PLL Bypass	0 (PLL active)
Phase Adjust		16
	Bit 7	0
VCO/CPMP	VCO Range	1
	Charge Pump Current	1

The Serial Port address for the AD9884 is 10011 xx0.



AD9884 Application Diagram

Pin Number	Name	Function
1,2,3,36,37,38,46,118	NC	No Connect (leave floating)
5,6,9,12,13,14,17,20,21,24,26,35,39,42,47,49, 51,52 53,63,73,83,93,103,113,119,121,122,123	GND	Ground
4,8,10,11,16,18,19,23,25,124,128	V_D	Converter Power Supply (nominally 3.3V)
7	R_{AIN}	Analog Input for Converter R
15	G_{AIN}	Analog Input for Converter G
22	B_{AIN}	Analog Input for Converter B
27	CKINV	Invert Sample Clock Input (2 pixels/clock mode)
28	CLAMP	Clamp Input(external CLAMP signal)
29	SDA	Serial Port Serial Data Input
30	SCL	Serial Port Serial Data Clock (400KHz maximum)
31	A_0	Serial Port Address Input 1
32	A_1	Serial Port Address Input 2
33,34,43,48,50	PV_D	PLL Power Supply (nominally 3.3V)
40	HSYNC	Horizontal SYNC Input
41	COAST	PLL COAST Signal Input
44	CKEXT	External Pixel Clock Input (to bypass internal PLL) or 10KΩ to V_{DD}
45	FILT	Connection for External Filter Components for Internal PLL
54,64,74,84,94,104,114,120	V_{DD}	Output Power Supply (nominally 3.3V)
55-62	D_BB_7-D_BB_0	Digital Outputs of Converter “B”, Channel B. D_BB_7 is the MSB.
65-72	D_BA_7-D_BA_0	Digital Outputs of Converter “B”, Channel A. D_BA_7 is the MSB.
75-82	D_GB_7-D_GB_0	Digital Outputs of Converter “G”, Channel B. D_GB_7 is the MSB.
85-92	D_GA_7-D_GA_0	Digital Outputs of Converter “G”, Channel A. D_GA_7 is the MSB.
95-102	D_RB_7-D_RB_0	Digital Outputs of Converter “R”, Channel B. D_RB_7 is the MSB.
105-112	D_RA_7-D_RA_0	Digital Outputs of Converter “R”, Channel A. D_RA_7 is the MSB.
115	DATACK	Data Output Clock
116	DATACK/	Data Output Clock Compliment
117	HSOUT	HSYNC Output Clock (phase-aligned with DATACK and DATACK/)
125	PWRDN/	Power Down and Three State Output Control (active low)
126	REFOUT	Internal Reference Output (bypass with .1µF to ground)
127	REFIN	Reference Input (+1.25V +/- 10%)

Application Diagram Notes:

1) All supply pins (V_D and V_{DD}) should be bypassed to the adjacent GND pin using 0.1uF chip capacitors as close to the pins as possible.

2) All GND pins should be tied to one common ground plane.

3) The user may consider making allowances to insert a series resistor in the data path (close to the AD9884) for additional isolation.

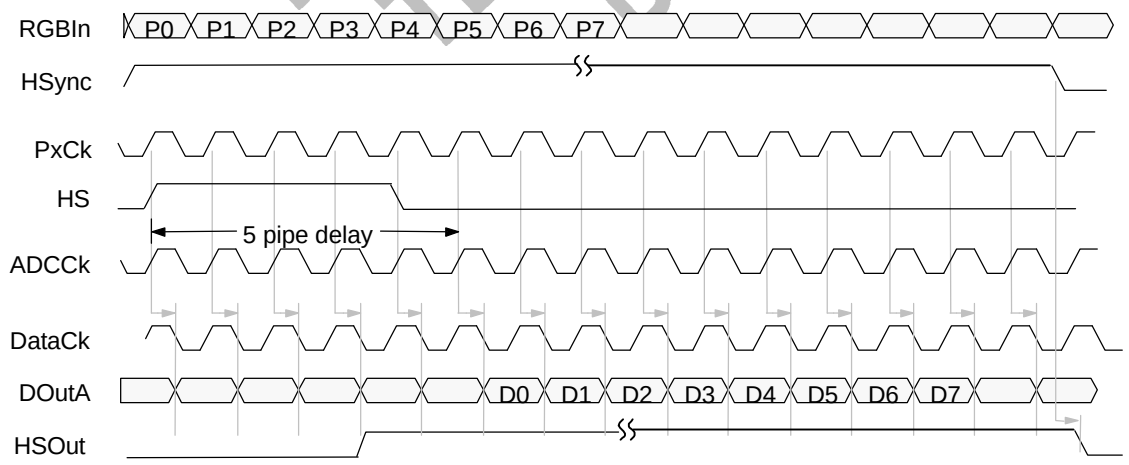
Timing Diagrams

The following timing diagrams show the operation of the AD9884 in all clock modes. The part establishes timing by having the sample that corresponds to the pixel digitized when the leading edge of HSYNC occurs sent to the "A" data port. In Dual Channel Mode, the next sample is sent to the "B" port. Future samples are alternated between the "A" and "B" data ports. In Single Channel Mode, data is only sent to the "A" data port.

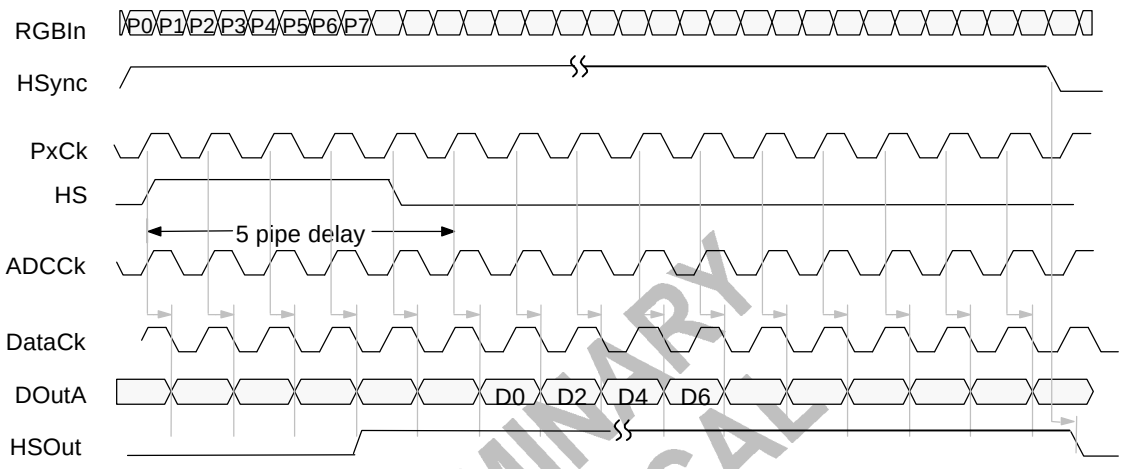
The Output Data Clock signal is created so that it's rising edge always occurs between "A" data transitions, and can be used to latch the output data externally. The HSYNC output is pipelined with the data in a fixed timing relationship between the two in all Single Channel modes (four data sets are presented before valid data is available) and in all Dual Channel modes (two data sets are presented before valid "A" port data is available).

In 2 pixels/clock modes, "even" pixels represent samples taken on the rising edge of the pixel clock (PXCK). "Odd" pixels represent samples taken on the falling edge of PXCK.

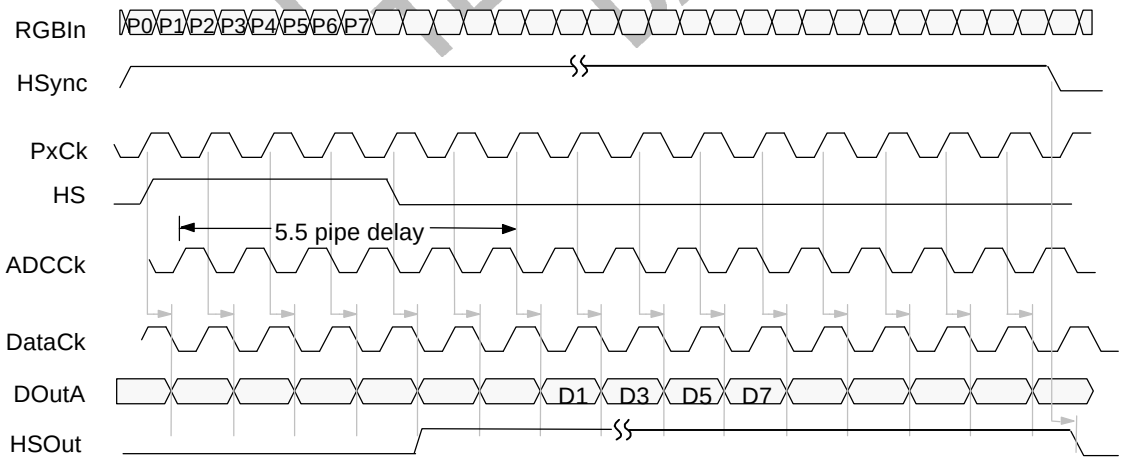
1. Single Channel Mode



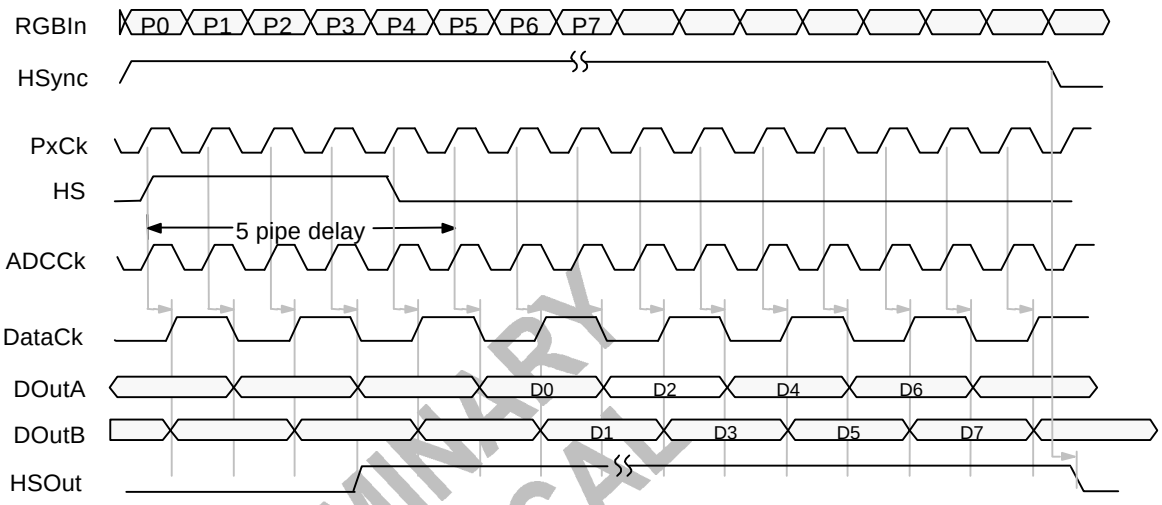
2. Single Channel Mode, 2 pixels/clock (even pixels)



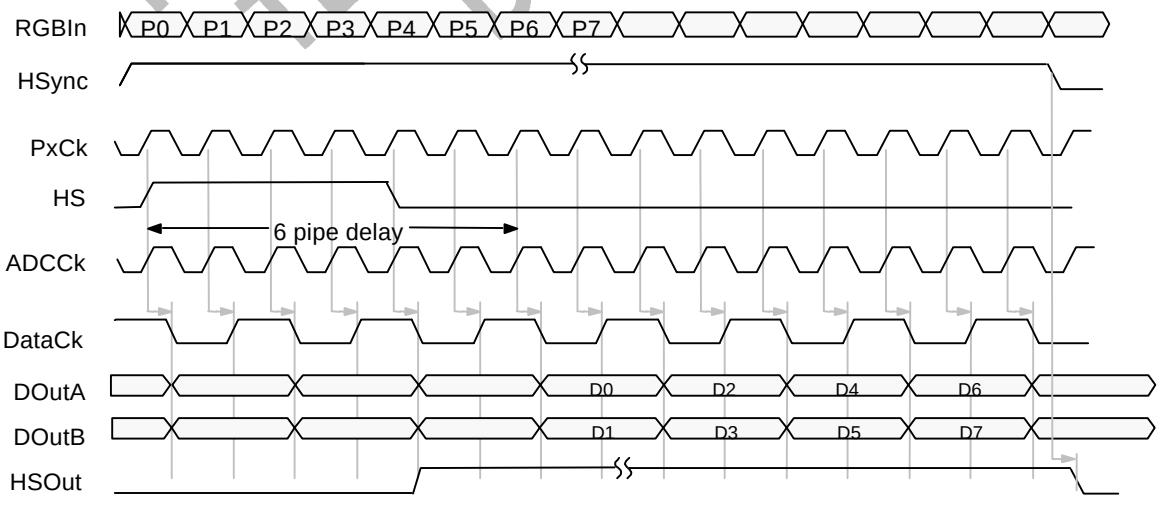
3. Single Channel Mode, 2 pixels/clock (odd pixels)



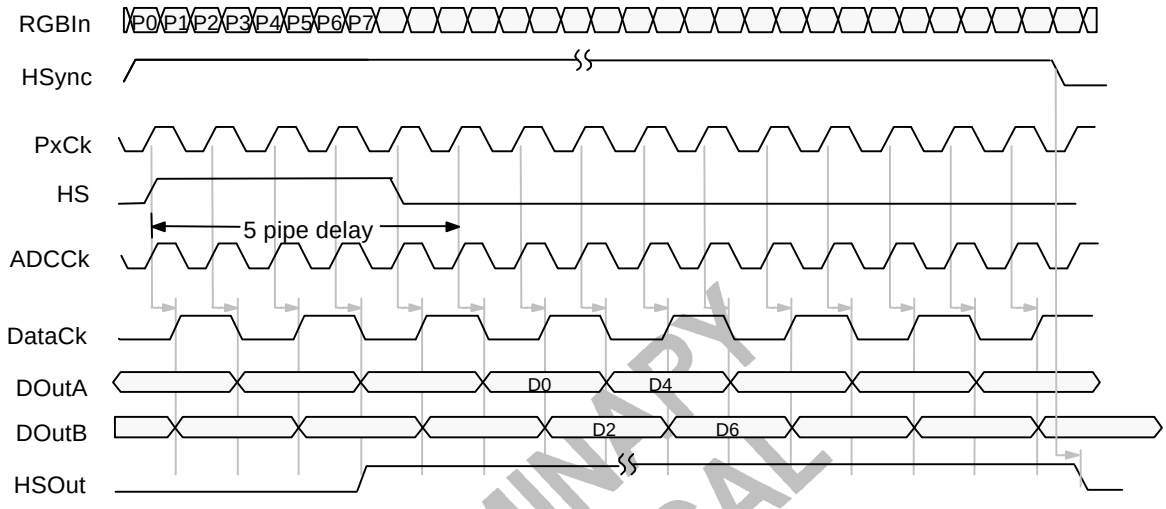
4. Dual Channel Mode, interleaved outputs



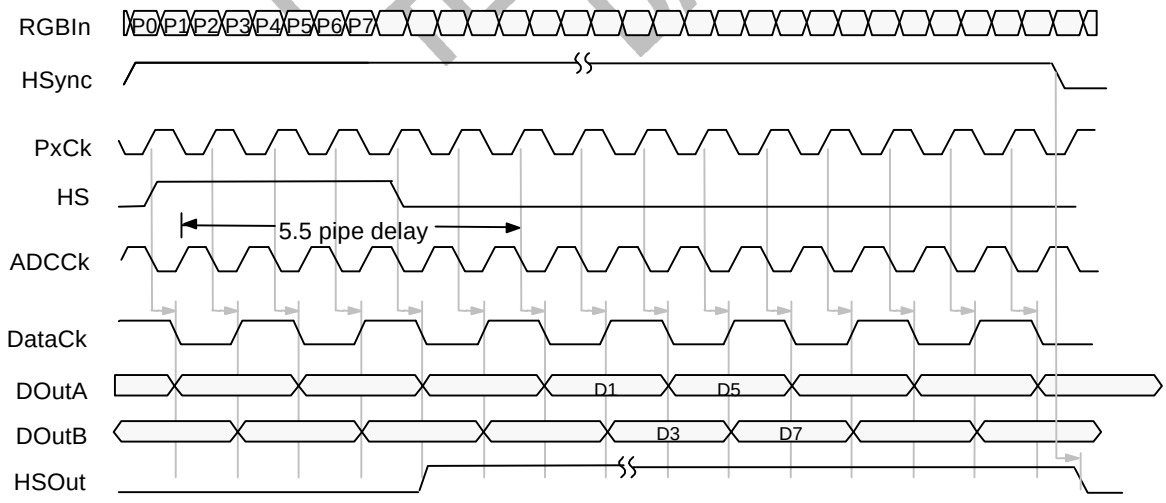
5. Dual Channel Mode, parallel outputs



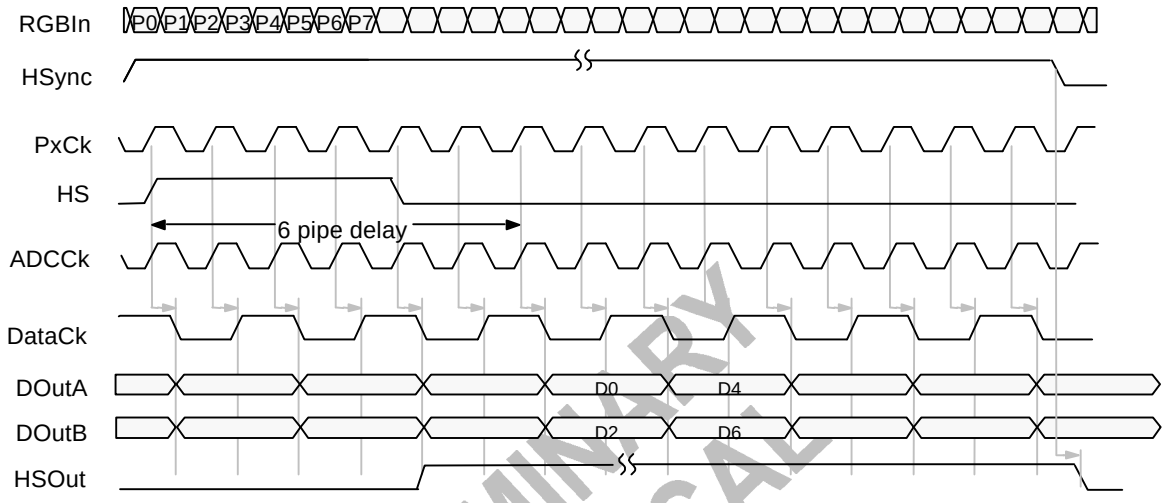
6. Dual Channel Mode, interleaved outputs, 2 pixels/clock (even pixels)



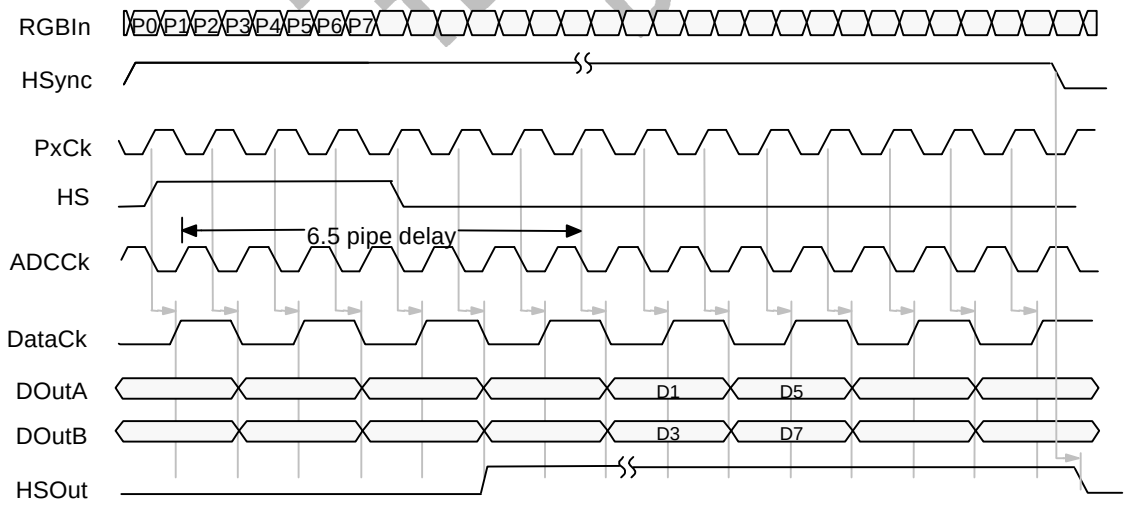
7. Dual Channel Mode, interleaved outputs, 2 pixels/clock (odd pixels)



8. Dual Channel Mode, parallel outputs, 2 pixels/clock (even pixels)



9. Dual Channel Mode, parallel outputs, 2 pixels/clock (odd pixels)



Clamp

The clamp signal is generated internally, or by the user through the CLAMP input pin. A 1-bit register loaded through the serial port controls the option of internal or external clamp. The polarity of the input clamp signal is programmable (also controlled by a 1-bit register loaded through the serial port.) External digital adjustment of the placement and duration of the CLAMP signal is controlled by two on-chip 8-bit registers. Leading edge placement of the internally generated clamp signal is relative to the trailing edge of HSYNC. The duration is relative to the leading edge of the generated clamp signal. The circuit contains two 8-bit counters clocked by the ADC clock, so 1 LSB of either placement or duration resolution is equal to a single ADC clock period.

Gain Control

The AD9884 has an analog input range of 0.5V to 1.0V. Gain on each channel is digitally adjustable through the 8-bit register. A gain setting of "0" corresponds to the minimum analog input range (0.5V p-p or less). A gain setting of 255 corresponds to the maximum analog input range (1V p-p or more).

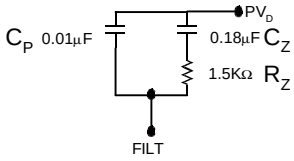
Offset Control

Each ADC channel is digitally adjustable for offset control through a 6-bit on-chip register. 1 LSB of offset equals 1 ADC LSB. An offset code setting of 31 means approximately zero offset. An offset setting code of 0 means approximately –31 codes of offset, and an offset setting of 63 means approximately 32 codes of offset at the ADC outputs.

Phase-Locked Loop

The PLL generates the appropriate pixel clock frequency from the incoming HSYNC signal. It is possible to bypass the PLL, providing the pixel clock externally through the CKEXT pin. Whether the pixel clock is taken from the PLL or the 1-bit PLL Bypass register controls the CKEXT pin. Setting PLL Bypass to `1' bypasses the PLL. If the pixel clock is being provided externally, the PLL is powered off.

An external low pass loop filter must be provided for the PLL to operate. This filter, which is connected to the FILT pin, is shown below with the required component values.



The loop filter component values together with charge pump current values serve to set the loop bandwidth and loop-damping coefficients. The loop equations for these parameters are

Loop natural frequency $\longrightarrow$ $\omega_n = \sqrt{\frac{K_{vco} I_p}{(C_z + C_p)N}}$; $\omega_z = \frac{1}{R_z C_z}$

Loop damping factor $\longrightarrow$ $\zeta = \frac{1}{2}\frac{\omega_n}{\omega_z}$.

Loop stability is achieved if $\omega_n < \frac{\omega_{in}}{10}$

Four programmable registers are provided to optimize the performance of the PLL. These registers are:

(1) The 12-bit Divisor Register. The input HSYNC frequencies range from 30 kHz to 90 kHz. The PLL multiplies the frequency of the HSYNC signal, producing output signal frequencies in the range of 20 MHz to 140 MHz. The Divisor Register controls the exact multiplication factor. This register may be set to any value between 221 and 4095. (The divide ratio that is actually used is the programmed divide ratio plus one.)

(2) The 3-bit VCO Range Register. To lower the sensitivity of the output frequency to noise on the control signal, the VCO operating frequency range is divided into four overlapping regions. The VCO Range register sets this operating range. Because there are only four possible regions, only the two least-significant bits of the VCO Range register are used. The frequency ranges for the lowest and highest regions are shown in Table 1.

Table 1: VCO Frequency Ranges

PV2	PV1	PV0	Range	K_{VCO} (Gain MHz/V)
1	0	0	20-60 MHz	100 MHz/V
1	0	1	50-90 MHz	100 MHz/V
1	1	0	80-120 MHz	135 MHz/V
1	1	1	110-140 MHz	160 MHz/V

(3) The 3-bit Pump Current Range register. This register allows the current that drives the low pass loop filter to be varied. The possible current values are listed in Table 2.

Table 2: Charge Pump Current/Control bits

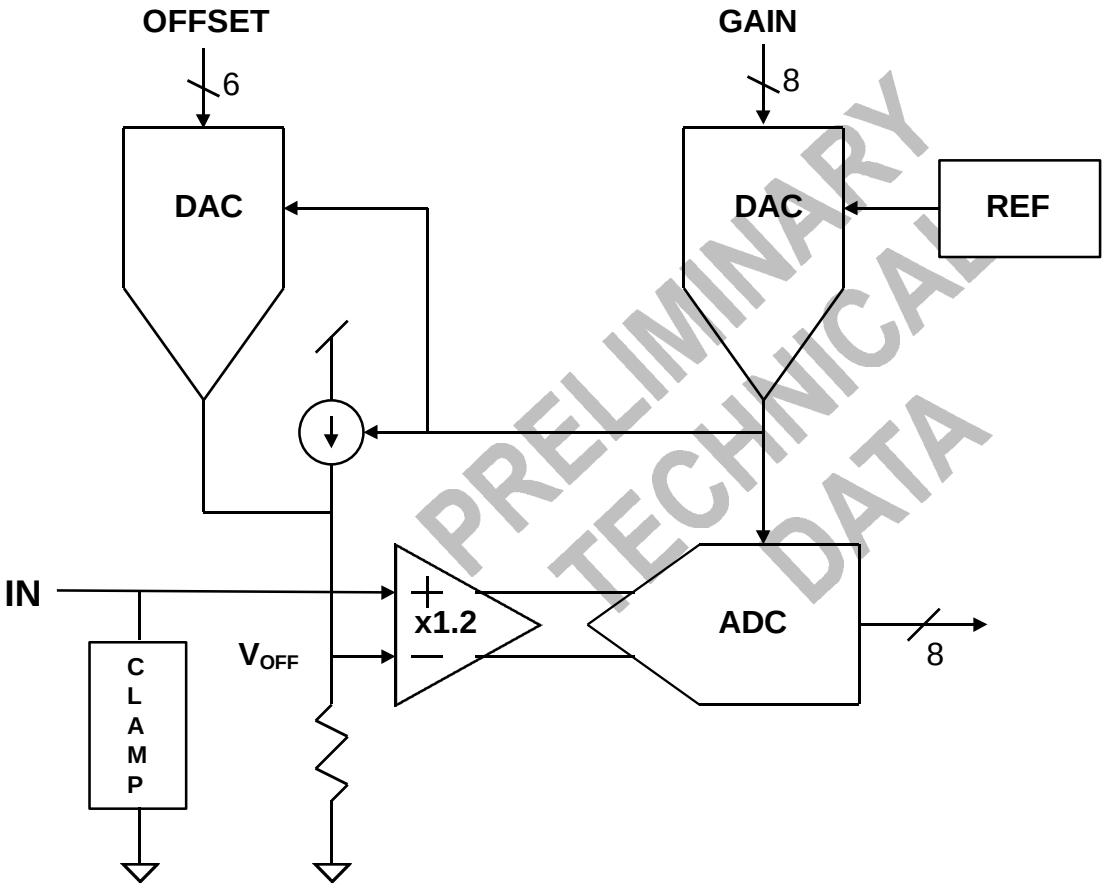
Ip2	Ip1	Ip0	Current (μA)
0	0	0	50
0	0	1	100
0	1	0	150
0	1	1	250
1	0	0	350
1	0	1	500
1	1	0	750
1	1	1	1500

(4) The 5-bit Phase Adjust Register. The phase of the generated sampling clock may be shifted to locate an optimum sampling point within a clock cycle. The Phase Adjust register provides 32 phase-shift steps of 11.25 degrees each. The HSYNC signal with an identical phase shift is available through the HSOUT pin. Phase adjustment is still available if the pixel clock is being provided externally.

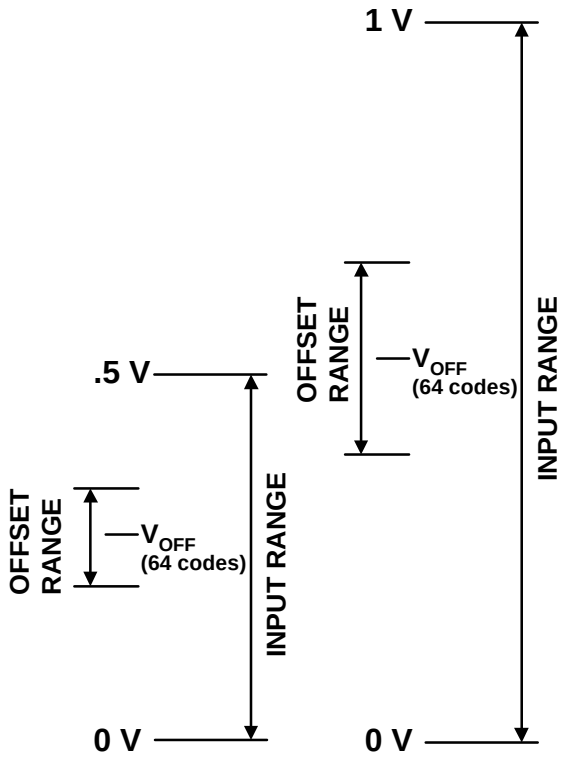
The COAST pin is used to allow the PLL to continue to run at the same frequency, in the absence of the incoming HSYNC signal. This may be used during the frame flyback, or any other time that the HSYNC signal is unavailable. The polarity of the COAST signal may be set through the Coast Polarity Register. Also, the polarity of the HSYNC signal may be set through the HSYNC Polarity Register. For both HSYNC and COAST, a value of `1' inverts the signal.

2 Pixels/Clock Mode

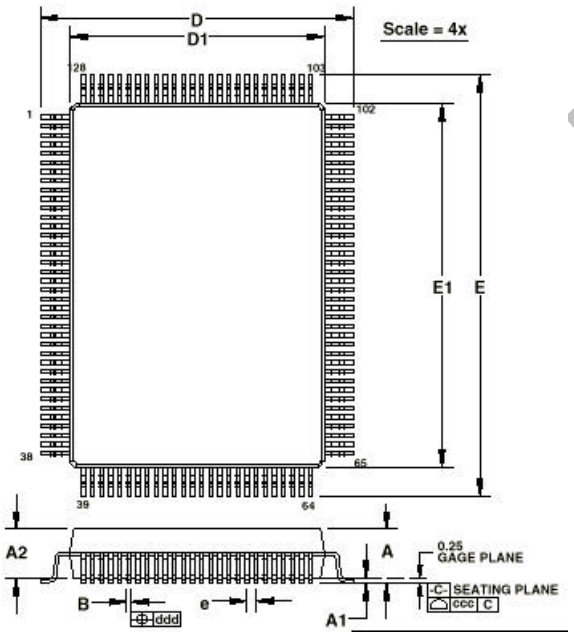
Logic 1 input on CKINV (pin 27) inverts the nominal ADC clock. Clock Invert can be switched between frames to implement the 2 Pixels/Clock Mode function. This allows higher effective image resolution to be achieved at lower pixel rates but with lower frame rates.



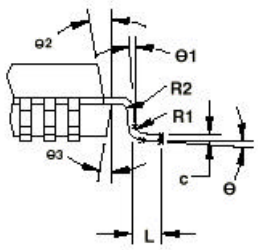
ADC Block Diagram (Single Channel Output)



Relationship of Offset Range to Input Range



Scale = 8x



Dim	Min.	Nom.	Max
A			3.40
A1	0.25		
A2	2.60	2.70	2.80
D	17.00	17.20	17.40
D1	13.90	14.00	14.10
E	23.00	23.20	23.40
E1	19.90	20.00	20.10
L	0.78	0.88	1.03
B	0.17	.22	0.27
e		0.50 BSC	
Θ	0°		7°
Θ1	2°	6°	10°
Θ2		10° TYP	
Θ3		10° TYP	
R1		0.30 RAD TYP	
R2		0.20 RAD TYP	
c			0.17
ddd			0.08
ccc			0.08

NOTES:

1. Controlling Dimensions are in mm.